

CLAIMS

What is claimed is:

1. A dielectric memory cell comprising:
 - a) a substrate comprising a source region, a drain region, and a channel region positioned there between;
 - b) a multilevel charge trapping dielectric positioned on the surface of the substrate; and
 - c) a control gate positioned on the surface of the multilevel charge trapping dielectric and positioned over and aligned with the channel region; and
 - d) wherein the multilevel charge trapping dielectric includes:
 - i) a tunneling dielectric layer adjacent to the substrate comprising a first dielectric material of a tunnel dielectric layer thickness;
 - ii) a top dielectric layer adjacent to the control gate comprising a second dielectric material of a top dielectric thickness which is less than the tunnel dielectric thickness;
 - iii) a charge trapping layer positioned between the tunneling dielectric layer and the top dielectric layer.

wherein the control gate has a control gate conduction band Fermi level and a control gate valance band Fermi level; and

wherein the difference between the control gate conduction band Fermi Level and a conduction band Fermi level of the top dielectric layer is less than the difference between the control gate valance band Fermi level and a valance band Fermi level of the top dielectric layer.
2. The dielectric memory cell of claim 1, wherein the control gate comprises polysilicon heavily implanted with a group III element.
3. The dielectric memory cell of claim 2, wherein the first dielectric material comprises silicon dioxide.

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4. The dielectric memory cell of claim 3, wherein the second dielectric material comprises silicon dioxide.
5. The dielectric memory cell of claim 4, wherein the charge trapping layer comprises a nitride compound.
6. The dielectric memory cell of claim 5 wherein the charge trapping layer is a nitride compound selected from the group of nitride compounds consisting of Si_2N_4 , Si_3N_4 , and SiO_xN_4 .
7. The dielectric memory cell of claim 6, wherein the second dielectric material is a dielectric selected from the group of an aluminum oxide compound, a Hafnium oxide compound, and a zirconium oxide compound.
8. The dielectric memory cell of claim 7, wherein the second dielectric material is a dielectric selected from the group of Al_2O_3 , HfSi_xO_y , HfO_2 , ZrO_2 , and ZrXi_xO_y .
9. The dielectric memory cell of claim 1, wherein the control gate comprises a material selected from a group of materials consisting of GaN, ZnS, and C; and wherein such material is heavily implanted with a group III element.
10. The dielectric memory cell of claim 9, wherein the first dielectric material comprises silicon dioxide.
11. The dielectric memory cell of claim 10, wherein the second dielectric material comprises silicon dioxide.
12. The dielectric memory cell of claim 11, wherein the charge trapping dielectric layer comprises a nitride compound.

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13. The dielectric memory cell of claim 12, wherein the charge trapping dielectric layer is a nitride compound selected from the group of nitride compounds consisting of Si_2N_4 , Si_3N_4 , and SiO_xN_4 .

14. The dielectric memory cell of claim 13, wherein the second dielectric material is a dielectric selected from the group of an aluminum oxide compound, a Hafnium oxide compound, and a zirconium oxide compound.

15. The dielectric memory cell of claim 14, wherein the second dielectric material is a dielectric selected from the group of Al_2O_3 , HfSi_xO_y , HfO_2 , ZrO_2 , and ZrXi_xO_y .

16. A charge trapping dielectric providing a non volatile storage of electrons in a dielectric memory cell, the charge trapping dielectric comprising:

- a) a tunneling dielectric layer adjacent to a substrate comprising a first dielectric material of a tunnel dielectric thickness;
- b) a top dielectric layer adjacent to a control gate comprising a second dielectric material having a top dielectric thickness, the top dielectric thickness being less than the tunnel dielectric thickness; and
- c) a charge trapping layer positioned between the tunneling dielectric layer and the top dielectric layer.

17. The charge trapping dielectric of claim 16, wherein the first dielectric material comprises silicon dioxide.

18. The charge trapping dielectric of claim 17, wherein the second dielectric material comprises silicon dioxide.

19. The charge trapping dielectric of claim 18, wherein the charge trapping layer comprises a nitride compound.

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20. The charge trapping dielectric of claim 19, wherein the charge trapping layer is a nitride compound selected from the group of nitride compounds consisting of Si_2N_4 , Si_3N_4 , and SiO_xN_4 .

21. The charge trapping dielectric of claim 20, wherein the second dielectric material is a dielectric selected from the group of an aluminum oxide compound, a Hafnium oxide compound, and a zirconium oxide compound.

22. The charge trapping dielectric of claim 21, wherein the second dielectric material is a dielectric selected from the group of Al_2O_3 , HfSi_xO_y , HfO_2 , ZrO_2 , and ZrXi_xO_y .